High-Q Capacitors Implemented in a CMOS Process for Low-Power Wireless Applications

Chih-Ming Hung, Yo-Chuol Ho, I-Chang Wu, and Kenneth O, *Member, IEEE*

***Abstract*—In a foundry 0.8-μm CMOS process, low-cost capacitors with a measured Q factor of around 50 at 3 GHz and high intrinsic capacitance/area ($\sim$200 nF/cm^2) were demonstrated. When extrapolated to 900 MHz, the Q factor is greater than 100. The capacitors use a poly-to-n-well MOS structure which has been commonly dismissed for high-Q applications due to the high n-well sheet resistance ($\sim 1\,\mathrm{k}\Omega/\square$). Utilizing the structure, a low-noise amplifier (LNA) with a resonant frequency of 960 MHz, power gain of 16.2 dB, 1-dB compression point ($P_{1\,\mathrm{dB}}$) of -5 dBm, and noise figure of 3.5 dB was demonstrated. Using a rule of thumb, the third-order harmonic intercept point (P_{IP3}) was estimated to be 5 dBm from the $P_{1\,\mathrm{dB}}$ data. Despite concerns for nonlinearity of the capacitors, these results suggest that this capacitor structure could be used in LNA's with a large dynamic range.**

***Index Terms*—CMOS, high-Q capacitor, quality factor, LNA, MOS capacitor.**

I. Introduction

CMOS technologies are showing promises for RF applications at 900 MHz and higher frequencies. One of the required passive components is an inexpensive, area-efficient, and high-quality (high-Q) factor capacitor which is easy to implement and utilize. The capacitors should also be linear and have low parasitic capacitance. To address this need, metal-to-metal capacitors with a Q factor of 80 at 2.5 GHz in a BiCMOS process [1] and polysilicon-to-n$^+$ plug capacitors in a bipolar process [2] have been discussed. The former structure suffers from a low capacitance/area and a relatively large parasitic capacitance, while the latter structure is not available in conventional foundry CMOS processes and requires additional processing steps. In this paper, using a conventional foundry 0.8-μm CMOS process, capacitors with a Q greater than 100 at 900 MHz and with a high intrinsic capacitance/area ($\sim$ 200 nF/cm^2) have been implemented. This was accomplished by optimizing layouts of a naturally available polysilicon-to-n-well MOS capacitor structure which has been commonly dismissed for RF applications due to the high n-well sheet resistance. To further demonstrate their usefulness for RF and microwave applications, the capacitor structure was utilized in a 3-V 900-MHz low-noise amplifier (LNA) similar to the LNA in [3] with excellent results.

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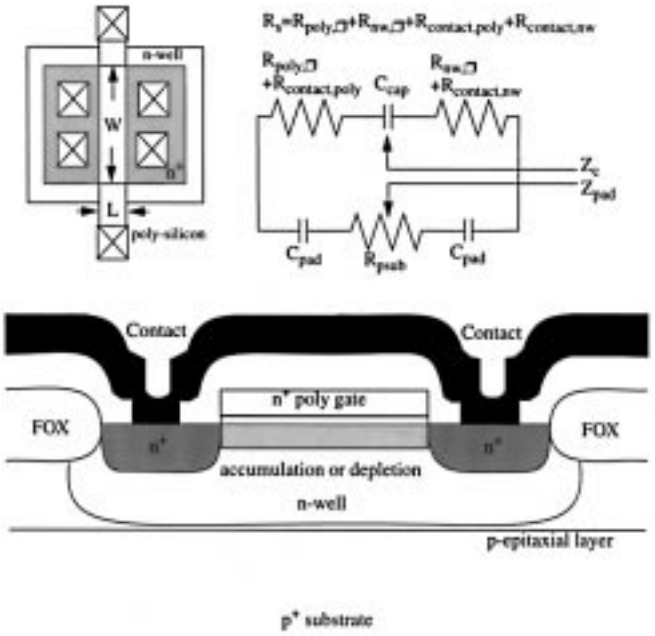
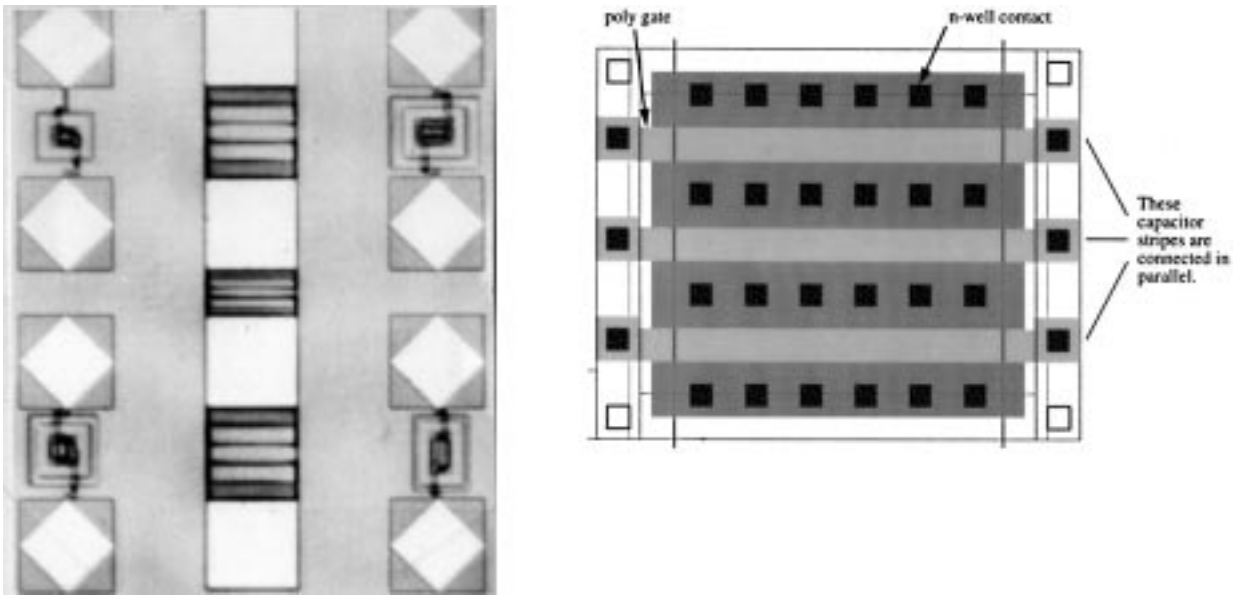


Fig. 1. A top view, cross section, and an equivalent circuit of the MOS capacitor structure.

II. Approach

Fig. 1 shows a top view, cross section, and an equivalent circuit model of a MOS capacitor test structure. Top and bottom plates of the capacitor are formed with silicided polysilicon and n-well, and are separated by a gate oxide (SiO_2) layer. C_{pad} and R_{psub} model parasitic capacitance and resistance associated with probe pads of the test structure. Since the gate oxide layer is very thin (thickness of $\sim$17 nm), the capacitor has a high intrinsic capacitance/area, especially if it is biased in the accumulation region [4]. Because of this, the structure can also have a high ratio between capacitance and parasitic capacitance associated with the n-well-to-substrate junction. If the capacitor is not biased in the accumulation, the capacitance will decrease by a factor of around two due to formation of a depletion region under the gate oxide [4]. The series resistance (R_s) originates from resistances of the silicided polysilicon gate ($R_{\mathrm{poly},\square}$, $\sim$2.3 $\Omega/\square$), n-well ($R_{\mathrm{nw},\square}$, $\sim$1.1 k$\Omega/\square$), vias, contacts (R_{cont}), and metal lines. Excluding the via, metal and contact resistances, and gate-bias dependence of the n-well resistance, the series resistance of the



(a) (b)

Fig. 2. (a) A capacitor microphotograph. (b) A high-Q capacitor layout. The area excluding contacts is $3 \times 1.2 \times 13.5\ \mu\text{m}^2$.

capacitors can be approximated as

$$R_S = \frac{1}{3} \times \frac{1}{2} \times \frac{1}{2} \times \frac{1}{N} \times \left(R_{\text{nw},\square} \times \frac{L}{W} + R_{\text{poly},\square} \times \frac{W}{L} \right) \tag{1}$$

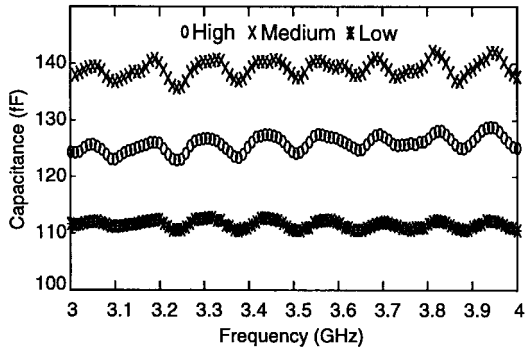
where N is the number of capacitor stripes, L and W are the length and width of the stripes (see Fig. 1), and $R_{\text{nw},\square}$ and $R_{\text{poly},\square}$ are the sheet resistances of the n-well and silicided polysilicon gate layer. The 1/3 factor accounts for the spreading effect while two 1/2 factors account for the double-sided contacts for the n-well and gate layers. For a required capacitance and thus a MOS capacitor area (A), N is equal to $A/(L \times W)$. Substituting this into (1), R_s can be expressed as a function of L and W as follows:

$$R_S = \frac{1}{12 \times A} \times (R_{\text{nw},\square} \times L^2 + R_{\text{poly},\square} \times W^2). \tag{2}$$

Since $R_{\text{nw},\square}$ is large compared to $R_{\text{poly},\square}$, the $R_{\text{nw},\square} \times L^2$ term typically dominates the total series resistance. To minimize R_s, the L needs to be as small as possible. Using (2), Q factors of the capacitors can be expressed as

$$Q = \frac{1}{\omega C R_s} = \frac{1}{\frac{\omega \times c_{\text{unit}}}{12} \times (R_{\text{nw},\square} \times L^2 + R_{\text{poly},\square} \times W^2)} \tag{3}$$

where ω is the frequency and c_{unit} is the intrinsic capacitance/area. When the minimum dimensions of L and W are used, the Q is the maximum. However, penalties are larger over all required area and n-well-to-substrate parasitic capacitance because of an increased number of contacts. As stated, the contact resistances are not included in the analysis since they are typically small. If needed, they can easily be included.



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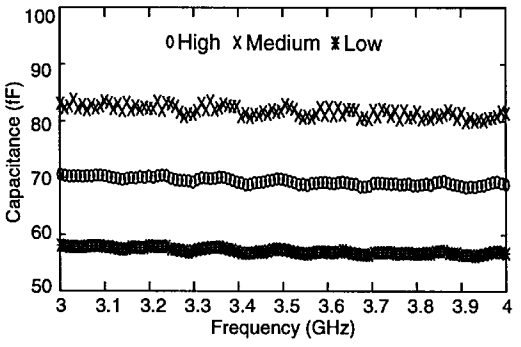
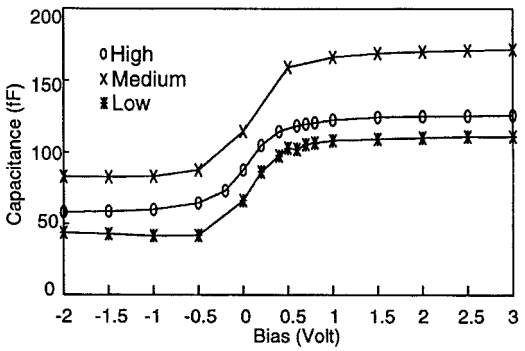


(b)

Fig. 3. Capacitance versus frequency (3-V top-plate bias). (a) Capacitance versus frequency plots of the high-, medium-, and low-Q capacitors. The variations are small over the 3–4-GHz frequency range. (b) Parasitic capacitance versus frequency plots of the high-, medium-, and low-Q capacitors. The variations are small over the frequency range between 3–4 GHz.



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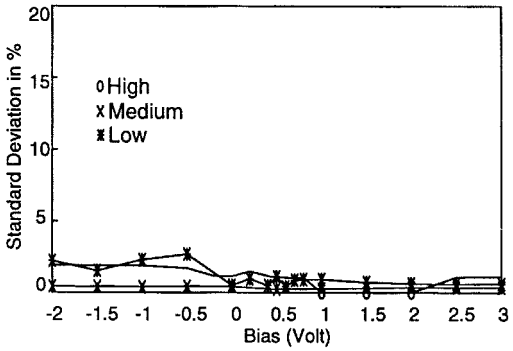
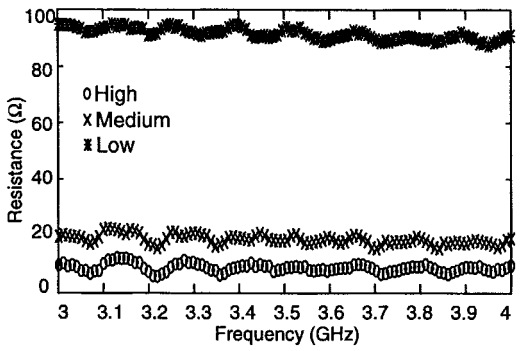


(b)

Fig. 4. (a) Capacitance versus bias voltage (average). High-frequency MOS C–V characteristics. For dc voltages greater than 1 V, the capacitors are quite linear. (b) Capacitance versus bias voltage (standard deviation). Standard deviation of the averaged capacitances versus bias plots for the high-, medium-, and low-Q capacitors. These low values indicate that the measurements are reliable.



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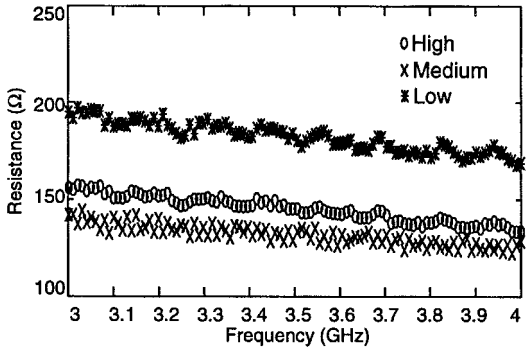


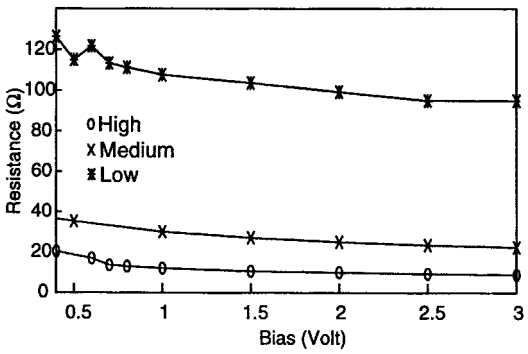
(b)

Fig. 5. (a) Extracted resistance versus frequency (poly-to-n-well capacitors at a 3-V top-plate bias. Measured resistance versus frequency plots of the high-, medium-, and low-Q capacitors. The variations are small over the 3–4-GHz frequency range. (b) Extracted resistance versus frequency (parasitic capacitors at a 0-V bias). Parasitic resistance versus frequency plots of the high-, medium-, and low-Q capacitors. The variations are small over the frequency range between 3–4 GHz.

In order to experimentally examine these, capacitor test structures were designed and fabricated. Capacitor values of ∼140 fF which are relatively small have been chosen to reduce impact of contact resistances between pads and microwave measurement probes. However, the small capacitor values introduced inconsistencies in capacitor measurements below around 2.5 GHz. Capacitor areas (excluding contact areas) were $3 \times 1.2 \times 13.6$ (48.9) μm^2 (High-Q), 2.4×24 (57.6) μm^2 (Medium-Q) and 9.2×5.6 (51.5) μm^2 (Low-Q). Fig. 2(a) shows a microphotograph of the capacitors, while Fig. 2(b) shows a layout of the high-Q capacitor.

III. Results and Discussion

One-port S-parameter data of the capacitors and open structures (pad frame) were collected using an HP8510C network analyzer. The S-parameter data were converted to admittances. To deembed effects of the pad frame, admittances of the open structures are subtracted from the measured total admittances since the pad parasitics are connected in parallel. Using the corrected admittance data (y_{11}), resistances and capacitances were then extracted from the real and imaginary parts, respectively. The measured MOS capacitances versus frequencies between 3–4 GHz are shown in Fig. 3(a) while the same for the parasitic n-well-to-substrate junction capacitances are shown in Fig. 3(b). The capacitance values were essentially constant over the frequencies between 3–4 GHz. Fig. 4(a) shows capacitances averaged over a frequency range between 3–4 GHz versus bias plots. The plots show the expected high-frequency C–V characteristics. For dc voltages greater than 1 V and lower than -0.5 V, the capacitors are quite linear. With proper biases, the capacitors can have a good linearity and a high intrinsic capacitance/area value. Standard deviations of the averaged capacitances in percent are shown in Fig. 4(b). The highest standard deviation of 2.7% indicates that the measurements are reasonable. Fig. 5(a) shows the series resistances of MOS capacitors measured at frequencies between 3–4 GHz and a 3-V bias. The resistances, like the capacitances, are essentially constant over the frequency range. Fig. 5(b) shows the resistance versus frequency plots for the parasitic capacitors. The extracted resistances decrease by ∼10% between 3–4 GHz. Averaged series resistances versus bias voltage between the tip and bottom plates for the MOS capacitors (over the same frequency range as the capacitances) are plotted in Fig. 6(a). Increasing the gate (top plate) bias voltage decreases the depletion layer width and increases the electron concentrations of the n-well under the gate region (accumulation), thus decreasing the n-well resistance. The resistances decreased by 30% to 40% depending on structures as the top-plate voltage was increased from 0.4 to 3 V. Standard deviations in percent are shown in Fig. 6(b). The standard deviations are less than 3% except for the high and



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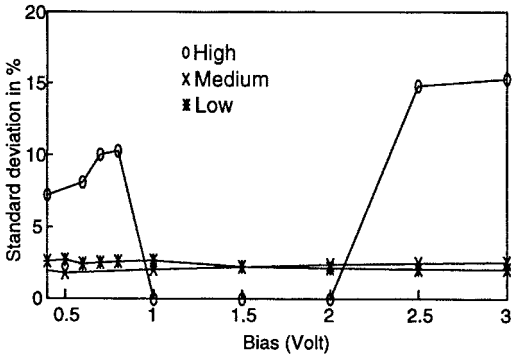
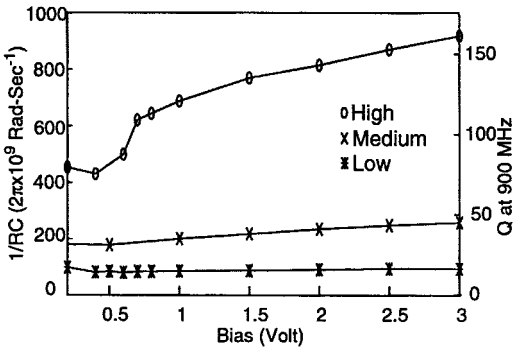


(b)

Fig. 6. (a) Resistance versus bias plots for poly-to-n-well capacitors (average). Resistance versus bias voltage plots for the high-, medium-, and low-Q capacitors. The electron concentration under the gate region increases with the bias voltage, thus reducing the resistance. (b) Resistance versus bias plots for poly-to-n-well capacitors (standard deviation). Standard deviation of the averaged resistances versus bias plots for the high-, medium-, and low-Q capacitors. The standard deviations are less than 3%, except for the high and low bias ranges of the high-Q capacitor, which indicates that the measurements are quite reasonable.



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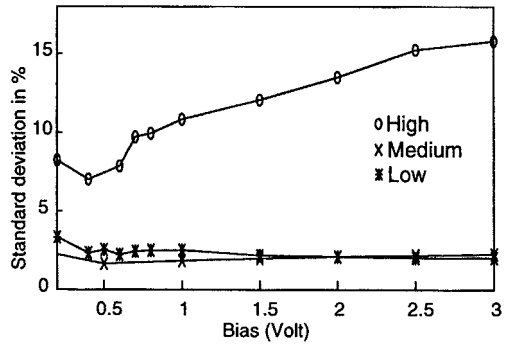


(b)

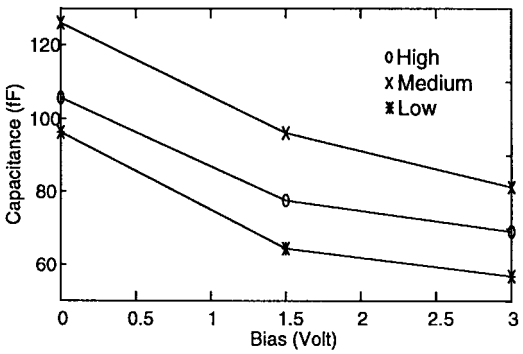
Fig. 7. (a) 1/*RC* versus vias voltage (average). Normalized Q factors (ωQ) and standard deviations versus bias plots of the high-, medium-, and low-Q capacitors. The ωQ was extracted by multiplying ω with $\mathrm{imag}(y_{11})/\mathrm{real}(y_{11})$. The Q values at 900 MHz were extrapolated using this ωQ. All the data were averaged over frequencies between 3–4 GHz. (b) 1/*RC* versus vias voltage (standard deviation). Standard deviations of the averaged ωQ.

low bias ranges of the high-Q capacitor, which implies that the measurements are reliable.

Q factors at 3 GHz were extracted using $\mathrm{imag}(y_{11})/\mathrm{real}(y_{11})$ definition and were 49, 14, and 5 for high-, medium-, and low-Q capacitors, respectively. Normalized Q factors ($1/RC$ or ωQ) are also extracted by multiplying ω and $\mathrm{imag}(y_{11})/\mathrm{real}(y_{11})$. The normalized Q factors as a function of bias are obtained once again by averaging over frequencies between 3–4 GHz for each bias. The Q values at 900 MHz were then extrapolated by dividing the normalized Q by $\omega = 2\pi \times 900$ MHz. Fig. 7(a) shows the normalized Q and extrapolated Q factors at 900 MHz versus bias. At a 3-V top-plate bias, the extrapolated Q values for the high-, medium-, and low-Q capacitors are 160, 46, and 17, respectively. If the contact and interconnect resistances between the capacitors and microwave probes were subtracted, the Q values would have been even higher. Standard deviations are shown in Fig. 7(b). Because the series resistance of the high-Q capacitor is small, data were noisier compared to those of the medium- and low-Q capacitors. Since the high-Q capacitor needs more contacts, the ratio between the capacitance and total capacitor area was lower. The ratios for the high-, medium-, and low-Q capacitors were 53, 73, and 88 nF/cm^2, respectively. These were low-end values since the design values of the capacitors were small. For larger high-Q capacitors, the capacitance–area ratio should approach 70 nF/cm^2, which are substantially higher than the metal-to-metal capacitors [1] and comparable to that of the polysilicon-to-n$^+$ plug capacitors [2].

Fig. 8(a) shows averaged capacitances versus bias plots for the n-well-to-substrate parasitic capacitors. As expected, the capacitances decrease with the bias voltage due to an increase in the depletion-layer width. They were relatively large due to unoptimized n-well layouts and small design values for the capacitors resulting in parasitic capacitances dominated by the perimeter components. When optimized, the ratios for the high-, medium-, and low-Q capacitors at a reverse junction voltage of 0.0 V should become around 2.4, 3, and 3, respectively. Of course, at a higher reverse junction voltage, the ratios will be higher. Fig. 8(b) shows standard deviation plots. The maximum standard deviation is $\sim$1%, which demonstrates consistency of the data.

Table I summarizes the measured resistances, capacitances, and Q factors [$\mathrm{Im}(y_{11})/\mathrm{Re}(y_{11})$] at 3 GHz, and extrapolated Q factor at 1 GHz for the MOS capacitors. The Q factors at 1 GHz were extrapolated by multiplying the 3-GHz data by a factor of 3. The measured parasitic capacitances associated with the n-well-to-substrate junction at 0- and 3-V biases are also listed in Table I. The table also lists estimated parasitic capacitances when the n-well layouts are optimized. The



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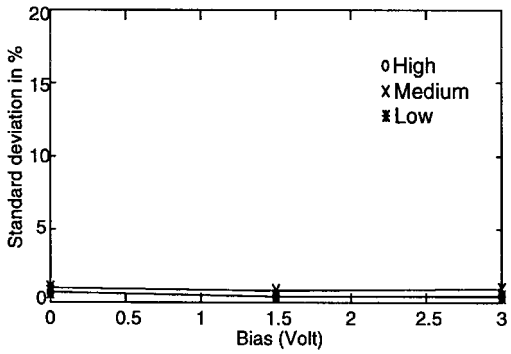


(b)

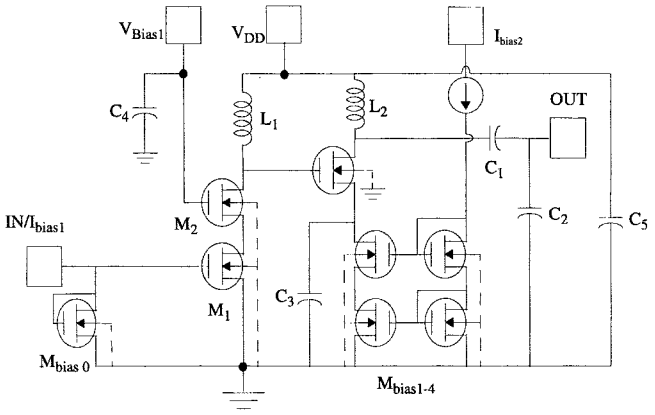
Fig. 8. (a) Parasitic capacitance versus bias voltage plots (average). Measured parasitic capacitances and standard deviations versus bias plots of the high-, medium-, and low-Q capacitors. The capacitance decreases with the n-well-to-substrate reverse junction voltage. (b) Parasitic capacitance versus bias voltage plots (standard deviation). Standard deviations of the averaged parasitic capacitances. The ~1% maximum deviation implies that the measurements are reliable.

TABLE I
SUMMARY OF CHARACTERISTICS OF MOS AND PARASITIC CAPACITORS

	MOS CAP.		PARASITIC CAP.			
	0.5V	3V	Measured Data (Ω, fF)		Opt. Cap. (fF)	
			0 V	3 V	0 V	3 V
High	R=19Ω C=116fF Q=24.22 @ 3GHz Q=72.66 @ 1GHz	R=9Ω C=126fF Q=47.2 @ 3GHz Q=141.6 @ 1GHz	R=179 C=106	R=140 C=69	53	37
Med	R=35Ω C=159fF Q=9.455 @ 3GHz Q=28.37 @ 1GHz	R=23Ω C=172fF Q=13.75 @ 3GHz Q=41.26 @ 1GHz	R=154 C=126	R=128 C=81	58	40
Low	R=116Ω C=103fF Q=4.43 @ 3GHz Q=13.29 @ 1GHz	R=92Ω C=112fF Q=5.14 @ 3GHz Q=15.42 @ 1GHz	R=197 C=96	R=176 C=57	38	27

parasitic capacitances of the optimized structures are around a half of the measured values. Furthermore, if the design values for capacitors are increased by 10×, the ratio of MOS to parasitic capacitance should increase by another factor of 2–3 due to the fact that as capacitor values are increased, the parasitic capacitance becomes dominated by the area rather than perimeter component.

Fig. 9(a) and (b) are a schematic and a microphotograph of a 3-V LNA utilizing the capacitors. The circuit consists



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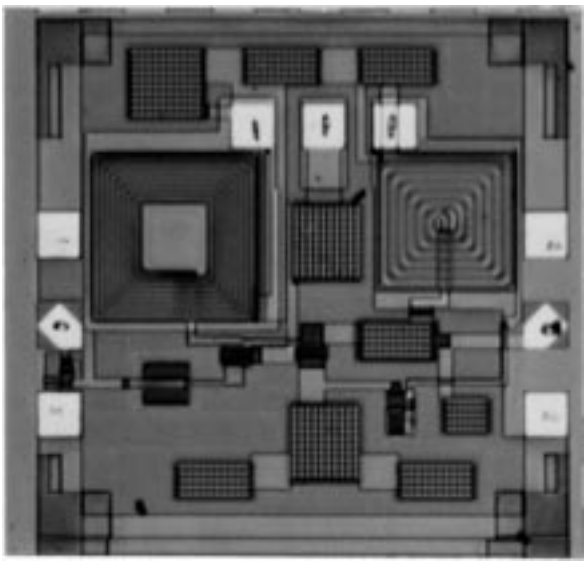

(b)

Fig. 9. (a) An LNA schematic. (b) An LNA microphotograph.

of two amplification stages, a capacitive transformer at the output, and bias circuitries. The transducer power gain and noise figure at the resonant frequency of 960 MHz were 16.2 and 3.5 dB, respectively. The second-stage biasing circuit is bypassed using a 40-pF MOS capacitor (C_3) to improve the stability. The top-plate voltage is ~1.4 V and the capacitor is in the accumulation region resulting in a high capacitance/area value. An output capacitor transformer is used for dc isolation and to improve the output matching with a negligible gain degradation. The values of C_1 and C_2 were 10.7 and 7.5 pF, respectively, and they were formed using MOS capacitors and associated parasitic capacitors. Top and bottom-plate dc biases of C_1 were ~2.7 and 0 V, respectively, while those of C_2 were 0 V. The 0-V dc bias on the bottom plate of C_1 is consistent with typical applications of the LNA in which it drives a passive filter. To investigate the linearity dependence on the gate bias of M_2, a pad for V_{bias1} is provided. A 20-pF capacitor (C_4) is included to bypass parasitic inductances and also to ac ground the gate of M_2. Lastly, a 20-pF capacitor (C_5) is used to bypass parasitic inductances associated with the supply and ground. Connecting the top plate to the supply and

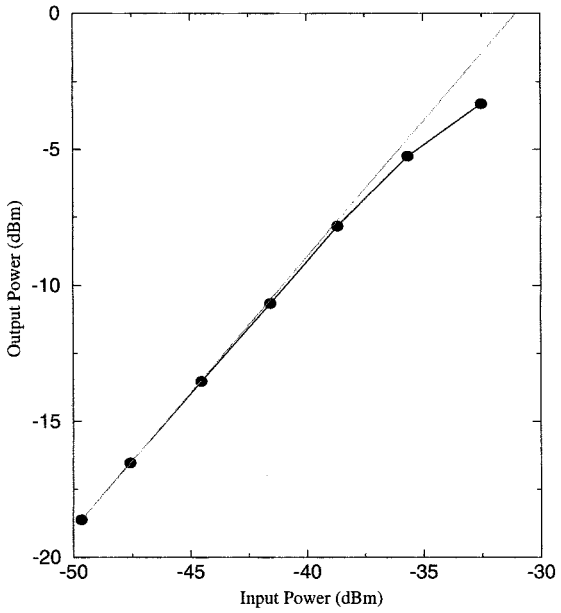

Fig. 10. An output power versus input power curve for the LNA. The $P_{1\,\mathrm{dB}}$ and P_{IP3} points are -5 and 5 dBm at the output.

the bottom to the ground ensures that the capacitor is biased in the accumulation. Fig. 9(b) clearly shows that a majority of the circuit area is occupied by inductors and capacitors, highlighting a need for area efficient capacitors and inductors.

A concern for the MOS capacitor structure and associated parasitic n-well-to-substrate junction capacitance is the linearity which can reduce the 1-dB compression ($P_{1\,\mathrm{dB}}$) (Fig. 10) and third-order intermodulation intercept (P_{IP3}) points of amplifiers. The measured $P_{1\,\mathrm{dB}}$ compression point of the LNA is around -5 dBm which should result a P_{IP3} of around 5 dBm (a rule of thumb [5]). The corresponding dynamic range for a 200-kHz channel is approximately 93 dB, while the spurious-free dynamic range is $\sim$69 dB, which are comparable to the previously reported bipolar LNA results [2].

IV. Conclusion

MOS capacitors with an extrapolated Q factor over 100 at 900 MHz were demonstrated using a conventional foundry CMOS process. Since the intrinsic capacitance is high and the MOS structures are naturally available in CMOS processes, the capacitors are area-efficient and inexpensive. Using the MOS capacitors, an LNA with a -5-dBm $P_{1\,\mathrm{dB}}$ compression point and an estimated P_{IP3} of around 5 dBm at the output was demonstrated. This suggests that despite concerns for nonlinearity and parasitic capacitances, the simple and inexpensive MOS capacitors should be suitable for GSM LNA applications. In addition, if the bias and operating range are properly selected, the capacitors can also be linear. Of course, it is unlikely that these capacitors can match characteristics of ceramic capacitors which have a Q of 2500–3000, low shunt parasitics, and small temperature dependences. However, for a wide range of applications such as bypassing, matching, and coupling which only require a Q factor of 10–100, this area-efficient and low-cost capacitor structure is well suited. Lastly, it should be reemphasized that to exploit this capacitor structure, care must be exercised to properly bias and reduce the substrate resistance.

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Dr. O has served as a member of the technical program committee for the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (1992, 1994), and in 1995 and 1996, he served as the short course chairman for the same conference. He was the recipient of the 1995 and 1997 IBM Faculty Development Awards, and the 1996 NSF Early Career Development Award.